

Linux perf_events status update

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Agenda

- New hardware support
- New kernel features
- Exploiting the uncore PMU on Intel servers
- Q&A



New hardware support

- Intel Haswell server (HSX) uncore in Linux v3.18
 - o memory controller, power, qpi, pcie, ...
- Intel Broadwell client (BDW, Xeon D) in Linux v4.1
 - o core PMU, power (RAPL), memory controller (IMC)
- Intel Broadwell SoC (Xeon D) uncore in Linux v4.2
 - memory controller, power, pcie
- Intel SkyLake client in Linux v4.3
 - o core PMU, includes new LBR, PEBS features



SkyLake new features

- Last Branch Buffer (LBR) has 32 entries (2x Haswell)
- Timed LBR: basic block cycle duration
 - capture cycle duration between consecutive branches
 - LBR record: 3x uint64 t now (50% increase)
- TSC is captured by PEBS
- PEBS precise Front-End sampling
 - sample where I-TLB, I-CACHE misses occur
- Patches by Andi Kleen (Intel) posted on LKML for Linux v4.3



LBR Call stack mode

- LBR records call branches and pops the last entry on return (Haswell)
 - o not work in certain corner cases; leaf call optimization
- Available in Linux v3.19
 - advantage: no framepointer, no dwarf needed, no user regs/stack snapshots
 - gotcha: only work in user mode (hw bug)
 - o new PERF SAMPLE BRANCH CALL STACK branch sample type
- perf tool integration
 - o perf record --call-graph lbr -e cycles: $uk... \Rightarrow user = lbr, kernel = FP$
 - \circ perf record --call-graph lbr -e cycles:k ... \Rightarrow error
 - o perf record --call-graph lbr -e cycles:u ... ⇒ lbr callstack
 - o reporting: perf report and naviguate the callstacks



Configurable Timestamp clock source

- Can configure the timestamp clock source per-event (Linux v4.0)
 - synchronize with user level generated samples from runtimes
 - was using kernel internal-only clock-source (sched_clock())
- perf_event_attr.clockid = N,.use_clockid = 1
 N is a POSIX clock identifier (MONOTONIC, REALTIME, RAW, ...)
- Example: correlate with Java JVMTI JIT information
 - JVMTI agent uses clock gettime (CLOCK MONOTONIC)
 - o perf event attr.clockid = CLOCK MONOTONIC
 - jit compiler events correlate automatically with perf samples

Sampling interrupt machine state

- Capture register state at PMU interrupt (Linux v3.19)
 - o can specify which registers to capture per event
- What is that useful for?
 - sampling value of registers at particular points
 - example: Am I calling memset () mostly with a size of 16?
- Value Profiling: sample values of function arguments
 - requires: reg-based calling convention (x86_64, ppc64, ...)
 - Intel x86: sample call instructions at target (1st instr of func) and save regs
 - o Intel x86: use br_inst_retired:near_call + pebs + skid \$ perf record -I -e cpu/event=0xc4, umask=0x2/p
 - visualization: perf report -D (for now),



Monitoring L3 cache occupancy

- Intel Cache Monitoring Technology (CMT)
 - Xeon specific feature, available on Haswell server
 - monitor L3 cache occupancy per process
- Available in Linux v4.2
 - can operate in per-thread and per-cpu mode incl. containers (cgroup)
 - o new PMU: intel cqm, new event: llc occupancy
 - o perf stat -I 1000 -e intel_cqm/llc_occupancy/ my_program
- Cache Allocation Technology (CAT)
 - enforce limits on L3 cache space (ways) available
 - patches posted on LKML by Intel



Cache monitoring examples (Haswell server)

perf stat -e intel cqm/llc occupancy/ -I 1000 ./triad

```
# time counts unit events
1.003202964 47185920.00 Bytes intel_cqm/llc_occupancy/
2.006316523 47480832.00 Bytes intel_cqm/llc_occupancy/

$ taskset -c 0 triad & taskset -c 18 triad &
$ # perf stat -a -e intel_cqm/llc_occupancy/ -I 1000 sleep 100
# time counts unit events
1.003116711 94371840.00 Bytes intel_cqm/llc_occupancy/
2.006269988 94371840.00 Bytes intel cqm/llc occupancy/
```

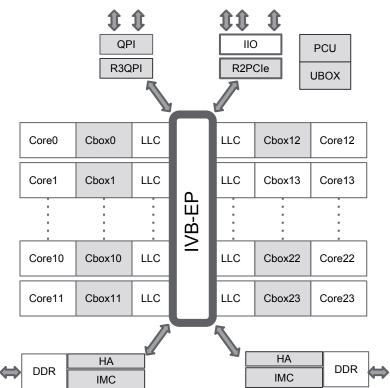
TSC, APERF, MPERF exposed!

- Provide a way to add free-running counters support
 - o free-running: non-stop, no-interrupt, fixed register
- Patch adds TSC, APERF, MPERF
 - APERF:increments in proportion to actual performance
 - MPERF: increments in proportion to a fixed frequency
 - ratio APERF/MPERF architecturally defined
- New freq PMU with new events: tsc, aperf, mperf
 - no sampling, no vmm
 - \$ perf stat -a freq/tsc/,freq/aperf/,freq/mperf/ -I 1000 sleep 10
- Just a proposal on LKML (Intel, Andy Lutomirski)



Exploiting uncore PMUs better in servers

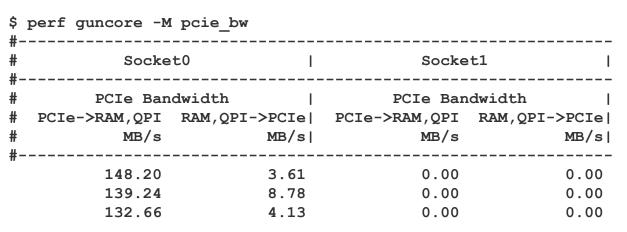
- Intel Xeon server have lots of PMUs
 - SNB-EP: 20, IVB-EP: 30, HSW-EP: 40
- Can monitor I/O, memory, power, inter-socket comm
- Each PMU has generic counters (+ some fixed)
- Only support system-wide measurements
- No sampling mode in perf_events
 - no interrupt (oftentimes)
 - o shared resources : cannot identify core
 - only sees physical addresses
- Kernel releases with support
 - SNB-EP: v3.6, IVB-EP: v3.10, HSW-EP: v3.18

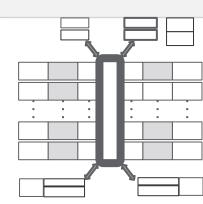




PCIe bandwidth (Intel IvyTown)

- L3 coherency agent PMU (Cbox) (uncore_cbox_*)
 - one Cbox agent per physical core
 - use TOR INSERTS event + opcode match PCle opcodes



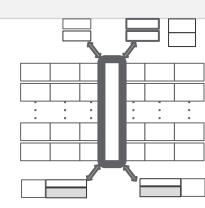




Memory bandwidth (IvyTown)

- Integrated Memory Controller (IMC) PMU (uncore_imc_*)
 - CAS_COUNT event to break down reads vs. write
- per-socket view useful to detect imbalance

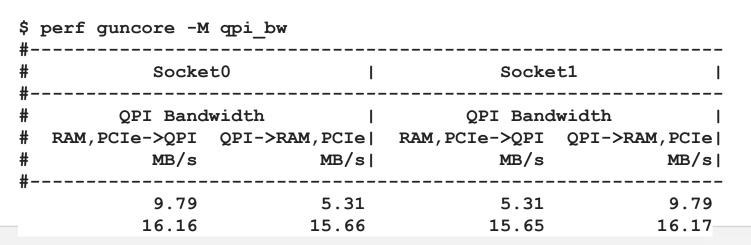
\$ p	erf guncore -M mem_bw			
# # #	Socket0	I	Socket1	l
# # # #	RAM Bandwidth Wr MB/s	 Rd MB/s	RAM Bandwidth Wr MB/s	 Rd MB/s
#	5.83 6.42	24.27 20.09	9.96 8. 4 0	15.35 15.75

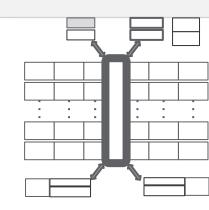




QuickPath Interconnect bandwidth

- QPI PMU (uncore_qpi_*)
 - RXL_FLITS and TXL_FLITS events
- detect remote socket accesses
- detect workload imbalance

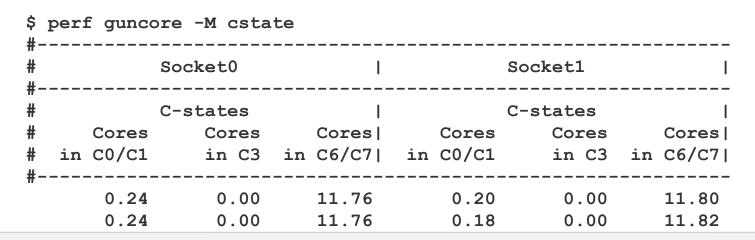


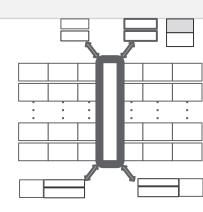




C-state monitoring

- Power Controller Unit (PCU) PMU (uncore pcu)
 - POWER STATE OCCUPANCY event
- useful to detect core utilization
- power saving opportunities







uncore view

- combining metrics to get a global view
 - question: Am I accessing remote memory?
 - perf guncore tool: mem_bw + qpi_bw

Socket0			1	Socket1			
 RAM Bandwidth		QPI Band	QPI Bandwidth RAM Bandwidth		I	QPI Bandwidth	
Wr	Rd	RAM, PCIe->QPI	QPI->RAM,PCIe	Wr	Rd	RAM, PCIe->QPI	QPI->RAM,PCIe
MB/s	MB/s	MB/s	MB/s	MB/s	MB/s	MB/s	MB/s
 6.75	19.40	6.57	4.85	8.97	20.78	4.84	6.58
5.91	21.69	9.71	3.43	9.07	17.78	3.43	9.71
4.46	17.14	5.68	2.29	6.39	15.48	2.29	5.68

Many more metrics possible, consult uncore programming guide



Intel Processor Tracing (PT)

- Hardware tracing support introduced with Broadwell processors
 - can trace control flow change in a compressed trace format
- kernel support via perf_events interface (Linux v4.1)
 - a lot of extensions to the sampling buffer (auxiliary buffer)
 - appears as new PMU: intel_pt
- perf tool support not quite complete in Linux 4.2
 - o perf record -e intel_pt//u ls
 - o perf report



Miscellaneous progress

- SandyBridge, IvyBridge, Haswell Hyperthreading counter corruption bug workaround
 - cross HT counter corruption with events 0xd0, 0xd1, 0xd2
 - sophisticated kernel workaround developed by Google
 - patch integrated into v4.1 (fixed in 4.2)
- perf JIT code profiling support
 - vastly benefit from the per-event clock source support
 - rebased to 3.19
 - still not merged in as of 4.3
 - needs some more cleanups based on LKML feedback
- IBM pushing Power8 Nest (uncore) support on LKML
 - Link, Memory bandwidth
 - Power



Conclusions

- Good progress this year
 - better set of features
 - stabilization and bug fixes
- SkyLake PMU looks very good
- Intel Cache Occupancy Monitoring is in
- Uncore PMU provides a wealth of useful information
- Intel Processor Trace is coming very soon now



References

- Intel official event tables
 - https://download.01.org/perfmon/
- Intel Cache Monitoring & Cache Allocation Technologies
 - <u>IA32 Software Developer's manual (SDM) Vol 3B</u> Chapter 17
 - CAT patch on LKML
- TSC/APERF/MPERF patch form LKML
- Intel Processor Trace (PT) support (Linux 4.1 + Broadwell processor)
 - Intel contribution (Adrian Hunter, Andi Kleen, Alexander Shishkin)
 - until fully merged, needs custom perf tool available on GitHUB <u>here</u>
- Intel uncore PMU guides
 - links to all guides available <u>here</u>
- IBM Nest patches